IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants

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PIPELINE ACCELERATOR HAVING MULTIPLE PIPELINE UNITS AND RELATED COMPUTING MACHINE AND **METHOD**

Serial Number

10/683,932

Filing Date:

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/ 2818

Attorney Docket No.:

1934-15-3

CERTIFICATE OF MAILING OR TRANSMISSION

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RULE 56 INFORMATION DISCLOSURE AND ACCOMPANYING SECTION 1.97(e) CERTIFICATION

TO THE COMMISSIONER FOR PATENTS:

In compliance with 37 CFR § 1.56 and § 1.97, Applicants acting by and through the attorney of record, hereby discloses patents and other documents listed on the attached Form PTO-1449 which may be considered relevant to the examination of the subject application.

A copy of the cited non-U.S. reference is enclosed.

Certification Under Section 1.97(e)

Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this statement.

Respectfully submitted,

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PTO/SB/08b(08-03)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known Application Number 10/683,932 Filing Date October 9, 2003 First Named Inventor Kenneth R. Schulz Art Unit 2818 Examiner Name 1934-15-3

(Use as many sheets as necessary)

of Attorney Docket Number Sheet

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T 2
		BAKSHI S; GAJSKI D D; "Partitioning and Pipelining for Performance-Constrained Hardware/Software Systems", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 7, NR. 4, PG. 419-432, (1999-12-00), XP000869229	
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